S/N 09/551027

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble Jr. et al.	Examiner:	Michael Trinh
Serial No.:	09/551027	Group Art Unit:	2822
Filed:	April 17, 2000	Docket:	303.379US2
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR		

INFORMATION DISCLOSURE STATEMENT

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE JR. ET AL.

By their Representatives,

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Date 1/5/04

By _____
Viet V. Tong
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5th day of January, 2004.

Amy Moriarty
Name

_____
Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/551027
Filing Date	April 17, 2000
First Named Inventor	Noble Jr., Wendell
Group Art Unit	2822
Examiner Name	Trinh, Michael
Attorney Docket No: 303.379US2	

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,570,176	02/11/1986	Kolwicz, K. D.	357	42	04/16/1984
	US-5,220,530	06/15/1993	Itoh, Masahiro	365	189.01	07/31/1991
	US-5,933,717	08/03/1999	Hause, Frederick N., et al.	438	200	03/04/1997
	US-6,016,268	01/18/2000	Worley, Eugene R.	365	149	02/05/1998
	US-6,242,775	06/05/2001	Noble, Wendell P.	257	330	02/24/1998
	US-6,433,382	08/13/2002	Orlowski, M , et al.	257	315	04/06/1995
	US-6,498,065	12/24/2002	Forbes, Leonard , et al.	438	259	08/30/2000
	US-6,528,837	03/04/2003	Forbes, L. , et al.	257	302	10/06/1997

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]
	JP-63066963	03/25/1988	Minegishi, K	H01L	27/10	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		WOLF, STANLEY , "Isolation Technolgies for Intergrated Circuits", Silicon Processing for the NLSI Era Vol. 2 Process Integration, (1990),66-78	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached